Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 8, 10, 16, and 17 have been amended. Claim 15 has been canceled. No claims have been added. Claims 4, 6, 18, and 20-24 were previously canceled. Therefore, claims 1-3, 5, 7-14, 16, 17, and 19 are presented for examination.

35 U.S.C. §103(a) Rejection

Claims 1-3, 5, and 7-19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Thomas et al. (U.S. Patent No. 5,752,011) in view of Shiell et al. (U.S. Patent No. 6,138,232). Applicant submits that the present claims are patentable over Thomas in view of Shiell.

Thomas discloses a method for controlling a processor's clock frequency to prevent overheating. Thomas attempts to maximize the processing speed of the processor while preventing overheating by monitoring a processor's activity and its temperature. When there is no activity for the processor, a slowed clock frequency is used, thereby saving power and lowering the thermal heat produced by the processor. When there is activity for the processor, a fast clock frequency is used. However, when prolonged activity (i.e., sustained fast clock frequency) causes the processor's temperature to become dangerously high for proper operation, the clock frequency is reduced to maintain processing speed at a reduced speed while preventing overheating. (See Thomas at Abstract.)

Shiell discloses a method of operating a microprocessor. The microprocessor accepts an interrupt from one of a plurality of interrupt sources. The microprocessor then operates at a rate dependent upon the interrupt source. The rate of power consumption by the

microprocessor corresponds to the selected rate of instruction operation. A rate table stores a table of interrupt source to rate of instruction operation. The rate table is accessed upon receipt of an interrupt to obtain a rate of instruction operation corresponding to the interrupt source. The microprocessor is then operated at the recalled rate. For a superscalar microprocessor capable of concurrently executing plural instructions simultaneously, the rate of instruction operation may be set by setting a number of instructions dispatched per instruction cycle. Electric power consumption is conserved by powering only those execution units to which instructions are dispatched. (See Shiell at col. 1, ll. 45 – col. 2, ll. 25.)

Claim 1, as amended, recites:

> A system comprising:
> a central processing unit (CPU);
> power management logic within the CPU to enable the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold;
> an artificial activity generator within the power management logic to generate artificial activity within the CPU whenever the temperature of the CPU is below the predetermined threshold to minimize current spikes within the CPU, the artificial activity being simulated instructions for the CPU; and
> programmable array logic (PAL) coupled to the CPU to operate as an interrupt handler to control the CPU upon receiving an interrupt from the power management logic indicating that temperature of the CPU is at least one of above or below the predetermined threshold.

Applicant submits that Thomas does not disclose or suggest an artificial activity generator within the power management logic to generate artificial activity within the CPU whenever the temperature of the CPU is below the predetermined threshold to minimize current spikes within the CPU, the artificial activity being simulated instructions for the CPU, as recited by claim 1. The Office Action cites the activity detector 68 of Thomas at

column 9, line 23 through column 10, line 2 as teaching this feature. (Office Action mailed 5/5/06 at pg. 2.) However, the activity generator 68 of Thomas only generates "a burst activity signal and a normal activity signal." (Thomas at col. 9, ll. 29-30.) There is no disclosure or suggestion in Thomas of the activity generator generating artificial activity, the artificial activity being simulated instructions for the CPU. Furthermore, there is no disclosure in Thomas of this artificial activity of simulated instructions being generated whenever the temperature of the CPU is below a predetermined threshold. As such, Thomas does not disclose or suggest an artificial activity generator within the power management logic to generate artificial activity within the CPU whenever the temperature of the CPU is below the predetermined threshold to minimize current spikes within the CPU, the artificial activity being simulated instructions for the CPU.

Applicant further submits that Shiell does not disclose or suggest an artificial activity generator within the power management logic to generate artificial activity within the CPU whenever the CPU is below the predetermined threshold to minimize current spikes within the CPU, the artificial activity being simulated instructions for the CPU. The Office Action does not rely on Shiell to disclose or suggest such a feature. Furthermore, applicant can find no disclosure or suggestion of this feature anywhere in Shiell. As such, Shiell does not disclose or suggest an artificial activity generator within the power management logic to generate artificial activity within the CPU whenever the temperature of the CPU is below the predetermined threshold to minimize current spikes within the CPU, the artificial activity being simulated instructions for the CPU.

As neither Thomas nor Shiell individually disclose an artificial activity generator within the power management logic to generate artificial activity within the CPU whenever

the CPU is below the predetermined threshold to minimize current spikes within the CPU, the artificial activity being simulated instructions for the CPU, any combination of Thomas and Shiell also does not disclose such a feature. Therefore, claim 1, as well as its dependent claims, is patentable over Thomas in view of Shiell.

Independent claims 8, and 16 also recite, in part, an artificial activity generator within the power management logic to generate artificial activity within the CPU whenever the CPU is below the predetermined threshold to minimize current spikes within the CPU, the artificial activity being simulated instructions for the CPU. As discussed above, Thomas in view of Shiell does not disclose or suggest such a feature. Therefore, claims 8 and 16, as well as their respective dependent claims, are patentable over Thomas in view of Shiell for the reasons discussed above with respect to claim 1.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: August 4, 2006

Ashley R. Ott
Reg. No. 55,515

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980